AMENDMENTS TO THE SPECIFICATION:

Please amend the title as follows:

--CIRCUIT FOR PROCESSING CHARGE DETECTING SIGNAL HAVING FETS WITH COMMONLY CONNECTED GATES--

Please cancel the originally-filed Abstract of the Disclosure an add the new Abstract which appears on a separate sheet in the Appendix.

Page 3, replace the paragraph beginning on line 24 and bridging pages 3 and 4 with the following amended paragraph:

--The thermal noises appearing at the output terminal Vout of the source follower circuit may be classified into the following three noises. The first type thermal noise (Vn1) is generated from the n-channel MOS field effect transistors in the source-follower circuit. The second type thermal noise (Vn2) appears at the output terminal Vout of the source-follower circuit upon input of a noise into the gate of the first enhancement type n-channel MOS field effect transistor 701 from the floating diffusion amplifier FDA. The third type thermal noise ~~(Vn2)~~ (Vn3) appears at the output terminal Vout of the source-follower circuit upon input of a noise into the gate of the second enhancement type n-channel MOS field effect transistor 702 from the second node "N2" as the output of the voltage dividing circuit. The first, second and third noises are caused from independent noise sources from each other. A noise voltage Vno caused by the thermal noise

appearing at the output terminal of the source follower circuit is given by:

$$Vno = \sqrt{(Vn1)^2 + (Vn2)^2 + (Vn3)^2} \quad ......(1)$$

where Vn1 is the first type thermal noise, Vn2 is the second type thermal noise, and Vn3 is the third type thermal noise. The first type thermal noise Vn1 is the noise generated from the source-follower circuit. The second type thermal noise ~~Vn1~~ Vn2 is the noise inputted into the source-follower circuit. Those noises are not directly relevant to the issue of the present invention.--

Page 5, replace the paragraph beginning on line 17 and bridging pages 5, 6 and 7 with the following amended paragraph:

--~~A~~ The third type thermal noise ~~voltage~~ Vn3 appearing at the output terminal Vout of the source follower circuit is caused by the noise voltage Vno2 which is generated from the voltage dividing circuit. FIG. 2 is a circuit diagram illustrative of a modified conventional source-follower circuit from the above first conventional source-follower circuit, wherein the noises are inputted into the gate of the second enhancement type n-channel MOS field effect transistor. A first enhancement type n-channel MOS field effect transistor 301 corresponds to the above first enhancement type n-channel MOS field effect transistor 701. A second enhancement type n-channel MOS field effect transistor 302 corresponds to the above second enhancement type n-channel MOS field effect transistor 702. The first enhancement type n-channel MOS field effect transistor 301 and the second

enhancement type n-channel MOS field effect transistor 302 are connected in series between the power voltage line VDD and the ground line GND. The first enhancement type n-channel MOS field effect transistor 301 is connected in series between the power voltage line VDD and the output terminal ~~Vn3~~ Vout. The second enhancement type n-channel MOS field effect transistor 302 is connected in series between the ground line GND and the output terminal ~~Vn3~~ Vout. The gate and drain of the first enhancement type n-channel MOS field effect transistor 301 is connected to the power voltage line VDD, wherein it is considered that the reset transistor turns ON and the gate of the first enhancement type n-channel MOS field effect transistor 301 has the same potential as the power voltage line VDD. The source of the first enhancement type n-channel MOS field effect transistor 301 is connected to the source follower output terminal ~~Vn3~~ Vout. The gate of the second enhancement type n-channel MOS field effect transistor 302 is connected to the second node. The drain of the second enhancement type n-channel MOS field effect transistor 302 is connected to the source follower output terminal ~~Vn3~~ Vout. The source of the second enhancement type n-channel MOS field effect transistor 302 is connected to the ground line. A noise inputted into the gate of the first enhancement type n-channel MOS field effect transistor 301 is ignored, whilst another noise inputted into the gate of the second enhancement type n-channel MOS field effect transistor 302 is considered. This circuit configuration is the

same as an n-channel MOS inverter circuit. ~~A~~ The noise voltage Vn3 appearing at the source-follower output terminal Vout is given by a product of the above second thermal noise voltage Vno2 of the dividing circuit and a gain of the n-channel MOS inverter. The n-channel MOS inverter shown in FIG. 2 has a gain Av. Assuming that a transmission conductance of the n-channel MOS field effect transistor is sufficiently larger than a transmission conductance caused by a substrate bias and also than a channel conductance caused by a channel modification effect, then the gain Va of the n-channel MOA inverter is given by:

$$Av = -(gm2/gm1) \quad ......(5)$$

where "gm1" is the transmission conductance of the first enhancement type n-channel MOS field effect transistor 301, and "gm2" is the transmission conductance of the second enhancement type n-channel MOS field effect transistor 302. The noise voltage Vn3 appearing at the source follower output terminal Vout and being caused by the thermal noise voltage Vno2 of the dividing circuit is given by:

$$Vn3 = \sqrt{[\{-(gm2/gm1)Vno2\}^2]} \quad ......(6)\text{--}$$

Page 18, replace the paragraph beginning on line 21 and bridging pages 18 and 19 with the following amended paragraph:

--Upon input of charge into the floating diffusion amplifier, a variation in potential of the first node N1 is ~~cased~~ caused. This variation in potential of the first node N1 causes a variation in potential of the gate of the first enhancement type

n-channel MOS field effect transistor 101 as the driver transistor. The source-follower circuit detects variation in potential. The depletion type n-channel MOS field effect transistor 103 as the reset transistor turns ON upon application of the reset pulses ϕ R into the gate thereof, so as to cause the potential of the first node N1 or the floating diffusion amplifier to correspond to the power voltage VDD. An input off-set voltage of the source-follower becomes equal to the power voltage VDD.--